**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings of claims in the application.

**Listing of Claims:**

1. (Currently Amended) A motherboard, comprising:

a chipset for managing data transfers within the motherboard;

a scalable interconnect connecting to the motherboard, said scalable interconnect supporting a number of interconnect lanes; and

a plurality of high-speed video card slots connected to the interconnect, the high speed video card slots including at least one first video card slot and second video card slot; and

a switch connected to said interconnect and adapted to convert the interconnect lanes into a plurality of distributed links such that there is a different one of said distributed links providing a connection to each of said plurality of high-speed video card slots,

wherein the motherboard enables a first and a second video card to attach, respectively, to the at least one first video card slot and second video card slot, and wherein the motherboard enables the first and the second video cards to operate in parallel to output graphics data to a single visual display device, and wherein said switch is configured to distribute lanes dynamically during operation <u>including data transmission</u> to said plurality of high-speed video card slots responsive to changes in bandwidth needs during processing by said video cards.

2. (Cancelled)

3. (Previously Presented) The motherboard of claim 1, wherein said interconnect comprises a x16 connection and said first and second high-speed video card slots are each physically configured as x16 video card slots, and wherein said switch dynamically distributes bandwidth from said x16 connection to said two x16 video card slots via said distributed links.

4. (Original) The motherboard of claim 1, wherein said interconnect comprises at least a x32 connection.

5. (Original) The motherboard of claim 4, wherein said interconnect is divided into two or more x16 connections between the chipset and the plurality of high-speed video card slots.

6. (Original) The motherboard of claim 1, wherein said interconnect comprises at least a x16 connection, and wherein said interconnect is divided into a x8 connection between the chipset and each of said plurality of high-speed video card slots.

7. (Previously Presented) The motherboard of claim 1, wherein said interconnect comprises a connection having at least 24 lanes, and wherein said switch dynamically distributes lanes at any given time during operation into a x8 connection between the chipset and one of said plurality of high-speed video card slots and a x16 connection between the chipset and another of said plurality of high-speed video card slots.

8-28. (Cancelled)

29. (Previously Presented) The motherboard of claim 1, wherein the switch allocates a first x16 connection to the first video card slot and a second smaller-scaled connection to the second video card slot.

30. (Original) The motherboard of claim 29, wherein the second connection is at least one of a x1, x2, x4, and x8 connection.

31. (Cancelled)

32. (Previously Presented) The motherboard of claim 1, further comprising a peripheral slot connected to the interconnect, wherein the first video card slot and the second video card slot have first prespecified dimensions and the peripheral slot has second prespecified dimensions, wherein the second dimensions differs from the first dimensions.

33. (Previously Presented) The motherboard of claim 1, wherein the first video card slot and the second video card slot have first prespecified dimensions and wherein the first dimensions of the video card slots are selected to allow a graphics card to be coupled to any of the video card slots.

34. (Original) The motherboard of claim 33, wherein the graphics card is designed to be used with a x16 connection.

35-40. (Cancelled)

41. (Currently Amended) A motherboard for supporting multiple video cards, the motherboard, comprising:

a processor socket adapted to receive a central processing unit (CPU);

a single scalable interconnect that provides data paths to the processor socket, said scalable interconnect supporting a number of interconnect lanes;

a plurality of high-speed video card slots connected to the interconnect, wherein each of the video card slots has first prespecified dimensions and is specifically adapted for coupling to a video card, card; and

a switch connected to said interconnect and adapted to convert the interconnect lanes into a plurality of distributed links such that there is a different one of said distributed links providing a connection to each of said plurality of high-speed video card slots,

wherein the motherboard is capable of receiving substantially similar first and second video cards and facilitating parallel operation of the first and [[a]] second video cards to output graphics data to a single visual display device, and wherein said switch is configured to distribute lanes dynamically during operation including data transmission to said plurality of high-speed video card slots responsive to changes in bandwidth needs during processing by said video cards.

42-43. (Cancelled).

44. (Previously Presented) The motherboard of claim 41, wherein each of the video card slots is configured to couple with a graphics card designed to be used with a x16 connection.

45. (Previously Presented) The motherboard of claim 41, wherein the interconnect and said switch produce a first data path and a second data path, each of the first and second data paths connecting the processor socket to different video

card slots, the first data path being equal to or larger in scale than the second data path.

46. (Original) The motherboard of claim 45, wherein the second data path comprises at least one of a x1, x2, x4, and x8 connection.

47. (Original) The motherboard of claim 41, further comprising a peripheral slot connected to the interconnect, the peripheral slot having different dimensions from the video card slots.

48. (Currently Amended) A high performance computer, comprising:

a motherboard including a CPU and scalable interconnect that supports a number of interconnect lanes, wherein the scalable interconnect connects to a first and a second high-speed video card slots via a switch, the first and second high-speed video card slots having [[have]] a substantially similar physical configuration, and wherein the video slot physical configuration is selected to allow the first and the second high-speed video card slots each to accept a graphics card;

a first graphics card coupled to the first high-speed video card slot; and

a second graphics card coupled to the second high-speed video card slot,

wherein the following occurs during operation <u>including data transmission</u> of said computer: said first and second graphics cards operate in parallel to output graphics data to a display device, said switch converts said interconnect lanes into two distributed links such that there is a different one of said distributed links connecting to each of said plurality of high-speed video card slots, and said switch distributes lanes to said distributed links in response to current bandwidth needs of said graphics cards during processing by said cards.

49. (Cancelled)

50. (Previously Presented) The motherboard of claim 1, wherein a display area of the display device is divided into first and second sections, said first video card performing graphics processing related to said first section; and said second video card performing graphics processing related to said second section.

51. (Previously Presented) The motherboard of claim 41, wherein a display area of the display device is divided into first and second sections, said first video card performing graphics processing related to said first section; and said second video card performing graphics processing related to said second section.

52. (Previously Presented) The computer of claim 48, wherein a display area of the display device is divided into first and second sections, said first video card performing graphics processing related to said first section; and said second video card performing graphics processing related to said second section.

53. (Previously Presented) The motherboard of claim 41, wherein said interconnect comprises a x16 connection and said high-speed video card slots are physically configured as x16 video card slots, and wherein said switch dynamically distributes bandwidth from said x16 connection to two x16 video card slots via said distributed links.

54. (Previously Presented) The motherboard of claim 41, wherein said interconnect comprises a connection having at least 24 lanes, and wherein said switch dynamically distributes lanes at any given time during operation into a x8 connection between the chipset and one of said plurality of high-speed video card

slots and a x16 connection between the chipset and another of said plurality of high-speed video card slots.

55. (Previously Presented) The computer of claim 48, wherein said interconnect comprises a x16 connection and said high-speed video card slots are physically configured as x16 video card slots, and wherein said switch dynamically distributes bandwidth from said x16 connection to said two x16 video card slots via said distributed links.

56. (Previously Presented) The computer of claim 48, wherein said interconnect comprises a connection having at least 24 lanes, and wherein said switch dynamically distributes lanes at any given time during operation into a x8 connection between the chipset and one of said plurality of high-speed video card slots and a x16 connection between the chipset and another of said plurality of high-speed video card slots.